

NB7V33M

1.8V / 2.5V, 10GHz ÷4 Clock Divider with CML Outputs

Multi-Level Inputs w/ Internal Termination

Description

The NB7V33M is a differential ÷4 Clock divider with asynchronous reset. The differential Clock inputs incorporate internal 50 Ω termination resistors and will accept LVPECL, CML and LVDS logic levels. The NB7V33M produces a ÷4 output copy of an input Clock operating up to 10 GHz with minimal jitter. The Reset pin is asserted on the rising edge. Upon powerup, the internal flip-flops will attain a random state; the Reset allows for the synchronization of multiple NB7V33M's in a system. The 16 mA differential CML output provides matching internal 50 Ω termination which guarantees 400 mV output swing when externally receiver terminated with 50 Ω to V_{CC}.

The NB7V33M is the ÷4 version of the NB7V32M (÷2) and is offered in a low profile 3 mm x 3 mm 16-pin QFN package.

The NB7V33M is a member of the GigaComm™ family of high performance clock products. Application notes, models, and support documentation are available at www.onsemi.com.

Features

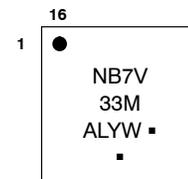
- Maximum Input Clock Frequency > 10 GHz, typical
- 260 ps Typical Propagation Delay
- 35 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV Peak-to-Peak, Typical
- Operating Range: V_{CC} = 1.71 V to 2.625 V with GND = 0 V
- Internal 50 Ω Input Termination Resistors
- Random Clock Jitter < 0.8 ps RMS
- QFN-16 Package, 3 mm x 3 mm
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

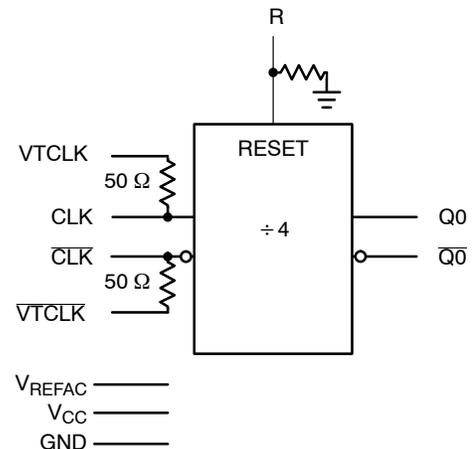


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

NB7V33M

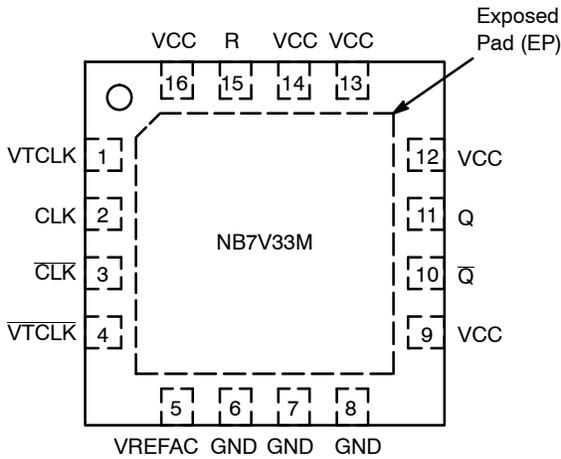


Figure 2. Pin Configuration (Top View)

Table 1. TRUTH TABLE

| CLK | CLK | R | Q | Q |
|-----|-----|---|---------|---------|
| x | x | H | L | H |
| Z | W | L | CLK ÷ 4 | CLK ÷ 4 |

Z = Low to High Transition
W = High to Low Transition
X = Don't Care

Table 2. PIN DESCRIPTION

| Pin | Name | I/O | Description |
|-----|--------|-------------------------|---|
| 1 | VTCLK | - | Internal 50 Ω Termination Pin for CLK |
| 2 | CLK | LVPECL, CML, LVDS Input | Non-inverted Differential CLK Input. Note 1. |
| 3 | CLK | LVPECL, CML, LVDS Input | Inverted Differential CLK Input. Note 1. |
| 4 | VTCLK | - | Internal 50 Ω Termination Pin for CLK |
| 5 | VREFAC | - | Internally Generated Output Voltage Reference for Capacitor-Coupled Inputs, Only |
| 6 | GND | - | Negative Supply Voltage |
| 7 | GND | - | Negative Supply Voltage |
| 8 | GND | - | Negative Supply Voltage |
| 9 | VCC | - | Positive Supply Voltage. Note 2. |
| 10 | Q | CML Output | Inverted Differential Output |
| 11 | Q | CML Output | Non-Inverted Differential Output |
| 12 | VCC | - | Positive Supply Voltage. Note 2. |
| 13 | VCC | - | Positive Supply Voltage. Note 2. |
| 14 | VCC | - | Positive Supply Voltage. Note 2. |
| 15 | R | LVC MOS Input | Asynchronous Reset Input. Internal 75 kΩ pulldown to GND. |
| 16 | VCC | - | Positive Supply Voltage. Note 2. |
| - | EP | - | The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board. |

1. In the differential configuration when the input termination pins (VTCLK/VTCLK) are connected to a common termination voltage or left open, and if no signal is applied on CLK/CLK input, then the device will be susceptible to self-oscillation. Q/Q outputs have internal 50 Ω source termination resistors.
2. All V_{CC} and GND pins must be externally connected to a power supply for proper operation.

NB7V33M

Table 3. ATTRIBUTES

| Characteristics | | Value |
|--|-----------------------------------|----------------------|
| ESD Protection | Human Body Model Machine Model | > 4 kV > 200 V |
| R_{PD} – Reset Input Pulldown Resistor | | 75 k Ω |
| Moisture Sensitivity (Note 3) | QFN16 | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | | 190 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------|--|--------------------|------------------|------------------------|---------------|
| V_{CC} | Positive Power Supply | GND = 0 V | | 3.0 | V |
| V_{IN} | Positive Input Voltage | GND = 0 V | | -0.5 to $V_{CC} + 0.5$ | V |
| V_{INPP} | Differential Input Voltage $ D - \bar{D} $ | | | 1.89 | V |
| I_{IN} | Input Current Through R_T (50 Ω Resistor) | | | ± 40 | mA |
| I_{OUT} | Output Current Through R_T (50 Ω Resistor) | | | ± 40 | mA |
| I_{VREFAC} | VREFAC Sink/Source Current | | | ± 1.5 | mA |
| T_A | Operating Temperature Range | | | -40 to +85 | $^{\circ}C$ |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | $^{\circ}C$ |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) (Note 4) | 0 lfpm 500 lfpm | QFN-16 QFN-16 | 42 35 | $^{\circ}C/W$ |
| θ_{JC} | Thermal Resistance (Junction-to-Case) (Note 4) | | QFN-16 | 4 | $^{\circ}C/W$ |
| T_{sol} | Wave Solder Pb-Free | | | 265 | $^{\circ}C$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

NB7V33M

Table 5. DC CHARACTERISTICS POSITIVE CML OUTPUT $V_{CC} = 1.71\text{ V to }2.625\text{ V}$; $GND = 0\text{ V}$; $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (Note 5)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|--|--|--|---------------|
| POWER SUPPLY CURRENT | | | | | |
| I_{CC} | Power Supply Current (Inputs and Outputs Open) $V_{CC} = 2.5\text{ V} \pm 5\%$ $V_{CC} = 1.8\text{ V} \pm 5\%$ | | 95 85 | 115 100 | mA |
| CML OUTPUTS | | | | | |
| V_{OH} | Output HIGH Voltage (Note 6) $V_{CC} = 2.5\text{ V}$ $V_{CC} = 1.8\text{ V}$ | $V_{CC} - 30$ 2470 1770 | $V_{CC} - 10$ 2490 1790 | V_{CC} 2500 1800 | mV |
| V_{OL} | Output LOW Voltage (Note 6) $V_{CC} = 2.5\text{ V}$ $V_{CC} = 1.8\text{ V}$ | $V_{CC} - 650$ 1850 $V_{CC} - 600$ 1200 | $V_{CC} - 550$ 1950 $V_{CC} - 500$ 1300 | $V_{CC} - 450$ 2050 $V_{CC} - 400$ 1400 | mV |
| DIFFERENTIAL INPUTS DRIVEN SINGLE-ENDED (Note 7) (Figures 5 & 6) | | | | | |
| V_{th} | Input Threshold Reference Voltage Range (Note 8) | 1050 | | $V_{CC} - 100$ | mV |
| V_{IH} | Single-ended Input HIGH Voltage | $V_{th} + 100$ | | V_{CC} | mV |
| V_{IL} | Single-ended Input LOW Voltage | GND | | $V_{th} - 100$ | mV |
| V_{ISE} | Single-ended Input Voltage ($V_{IH} - V_{IL}$) | 200 | | 1200 | mV |
| VREFAC | | | | | |
| V_{REFAC} | Output Reference Voltage @100 μA for Capacitor- Coupled Inputs, Only $V_{CC} = 2.5\text{ V}$ $V_{CC} = 1.8\text{ V}$ | $V_{CC} - 850$ $V_{CC} - 750$ | | $V_{CC} - 500$ $V_{CC} - 450$ | mV |
| DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 7 & 8) (Note 9) | | | | | |
| V_{IHD} | Differential Input HIGH Voltage | 1100 | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage | GND | | $V_{CC} - 100$ | mV |
| V_{ID} | Differential Input Voltage ($V_{IHD} - V_{ILD}$) | 100 | | 1200 | mV |
| V_{CMR} | Input Common Mode Range (Differential Configuration, Note 10) (Figure 9) | 1050 | | $V_{CC} - 50$ | mV |
| I_{IH} | Input HIGH Current ($V_{Tx}/\sqrt{T_x}$ Open) | -150 | | 150 | μA |
| I_{IL} | Input LOW Current ($V_{Tx}/\sqrt{T_x}$ Open) | -150 | | 150 | μA |
| CONTROL INPUT (Reset pin) | | | | | |
| V_{IH} | Input HIGH Voltage for Control Pin | $V_{CC} - 200$ | | V_{CC} | mV |
| V_{IL} | Input LOW Voltage for Control Pin | GND | | 200 | mV |
| I_{IH} | Input HIGH Current | -150 | | 150 | μA |
| I_{IL} | Input LOW Current | -150 | | 150 | μA |
| TERMINATION RESISTORS | | | | | |
| R_{TIN} | Internal Input Termination Resistor | 45 | 50 | 55 | Ω |
| R_{TOUT} | Internal Output Termination Resistor | 45 | 50 | 55 | Ω |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V_{CC} .
- CML outputs loaded with $50\text{-}\Omega$ to V_{CC} for proper operation.
- V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.
- V_{th} is applied to the complementary input when operating in single-ended mode.
- V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.
- V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

NB7V33M

Table 6. AC CHARACTERISTICS $V_{CC} = 1.71\text{ V to }2.625\text{ V}$; $GND = 0\text{ V}$; $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (Note 11)

| Symbol | Characteristic | Min | Typ | Max | Unit | |
|--------------------------|---|--|--|--|----------------------|----|
| f_{MAX} | Maximum Input Clock Frequency | 10 | 11 | | GHz | |
| V_{OUTPP} | Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \leq 10\text{ GHz}$ (Note 12) (Figure 3) | 260 | 400 | | mV | |
| t_{PLH} , t_{PHL} | Propagation Delay to Differential Outputs, @ 1 GHz, measured at differential crosspoint | CLK/ \overline{CLK} to Q, \overline{Q} R to Q, \overline{Q} | 150 500 | 200 600 | 350 700 | ps |
| $t_{PLH\ TC}$ | Propagation Delay Temperature Coefficient | | 50 | | $\Delta fs/^\circ C$ | |
| t_{skew} | Duty Cycle Skew (Note 13) Device – Device skew ($tpdmax - tpdmin$) | | | 20 50 | ps | |
| t_{RR} | Reset Recovery (See Figure 16) | 550 | 135 | | ps | |
| t_{PW} | Minimum Pulse Width R | 500 | 200 | | ps | |
| t_{DC} | Output Clock Duty Cycle (Reference Duty Cycle = 50%) $f_{in} \leq 10\text{ GHz}$ | 45 | 50 | 55 | % | |
| ϕ_N | Phase Noise, $f_c = 1\text{ GHz}$ | | 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz 40 MHz | -144 -147 -152 -152 -152 -153 | dBc | |
| $t_{j\phi N}$ | Integrated Phase Jitter (Figure x) $f_c = 1\text{ GHz}$, 12 kHz – 20 MHz Offset | | 35 | | fs | |
| t_{JITTER} | RJ – Output Random Jitter (Note 14) $f_{in} \leq 10.0\text{ GHz}$ | | 0.2 | 0.8 | ps RMS | |
| V_{INPP} | Input Voltage Swing (Differential Configuration) (Figure 11) (Note 15) | 200 | | 1200 | mV | |
| t_r , t_f | Output Rise/Fall Times @ 1 GHz (20% – 80%), Q, \overline{Q} | 20 | 35 | 60 | ps | |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Measured using a 1 GHz, $V_{INPPmin}$, 50% duty-cycle clock source. All output loading with external 50 Ω to V_{CC} . Input edge rates 40 ps (20% – 80%).
12. Output voltage swing is a single-ended measurement operating in differential mode.
13. Duty cycle skew is defined only for differential operation when the delays are measured from cross-point of the inputs to the cross-point of the outputs. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw-} and T_{pw+} @ 1 GHz. Skew is measured between outputs under identical transitions and conditions.
14. Additive RMS jitter with 50% duty cycle clock signal.
15. Input voltage swing is a single-ended measurement operating in differential mode.

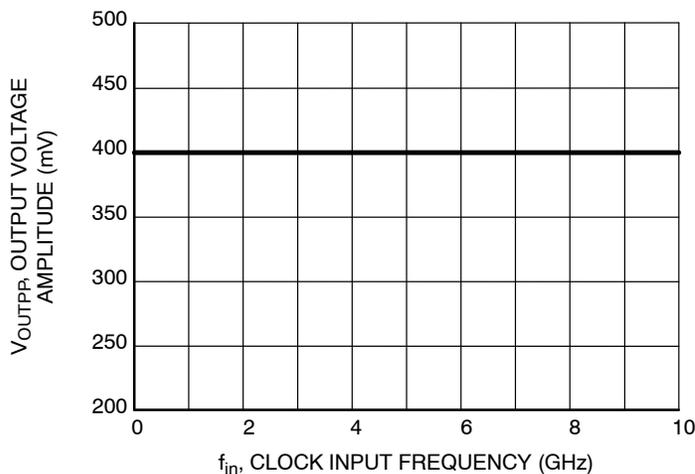


Figure 3. Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

NB7V33M

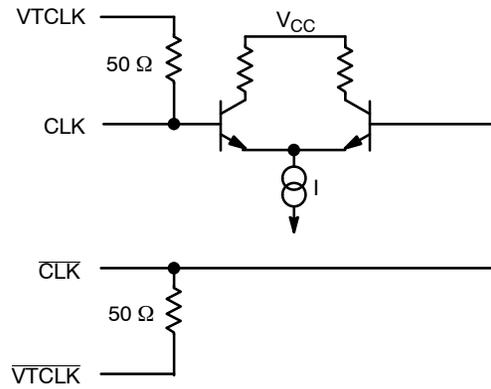


Figure 4. Input Structure

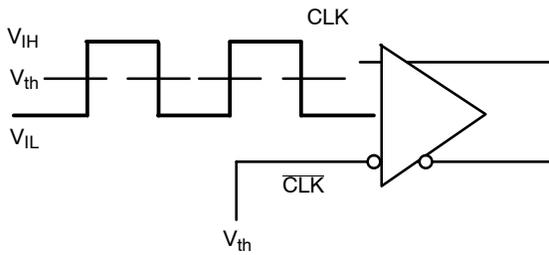


Figure 5. Differential Input Driven Single-Ended

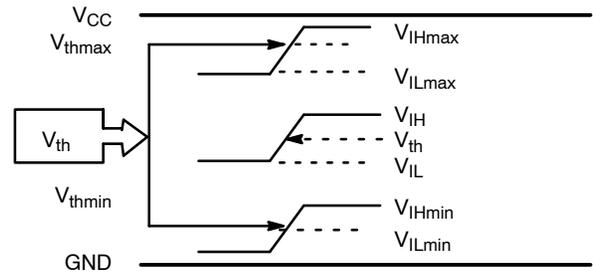


Figure 6. V_{th} Diagram

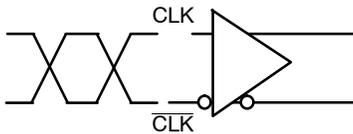


Figure 7. Differential Inputs Driven Differentially

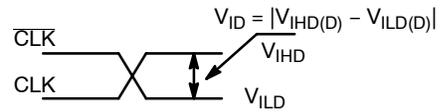


Figure 8. Differential Inputs Driven Differentially

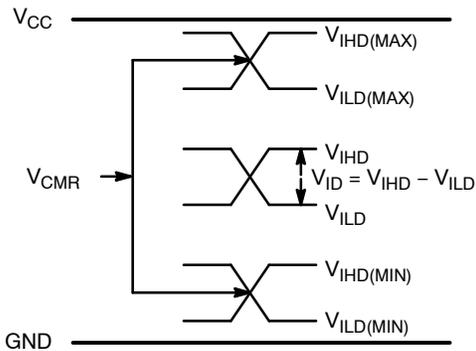


Figure 9. V_{CMR} Diagram

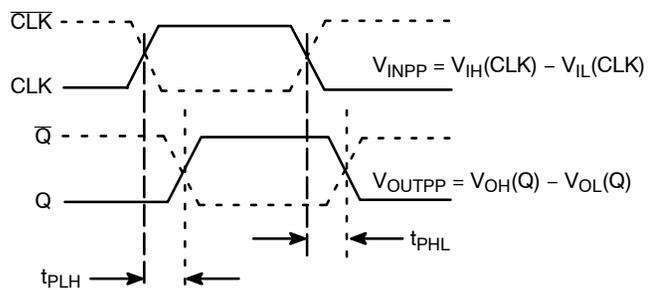


Figure 10. AC Reference Measurement

NB7V33M

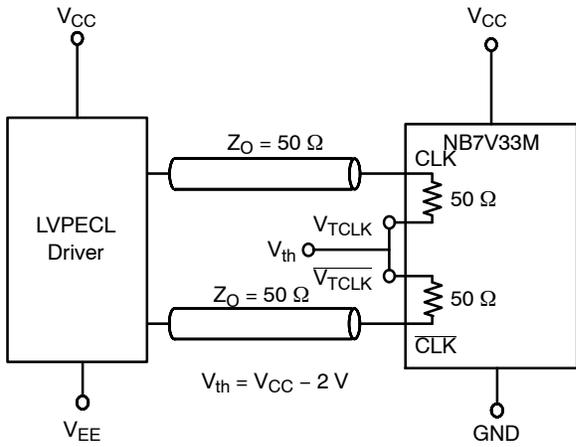


Figure 11. LVPECL Interface

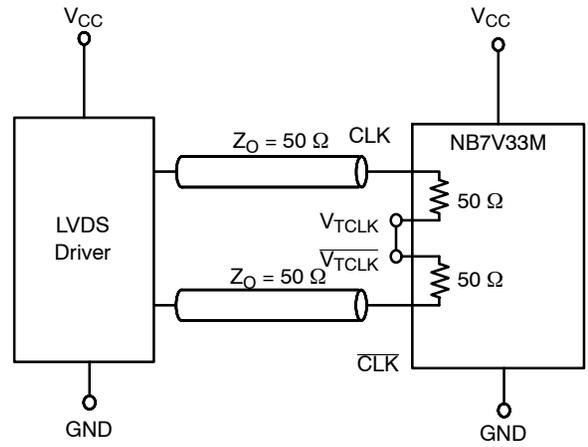


Figure 12. LVDS Interface

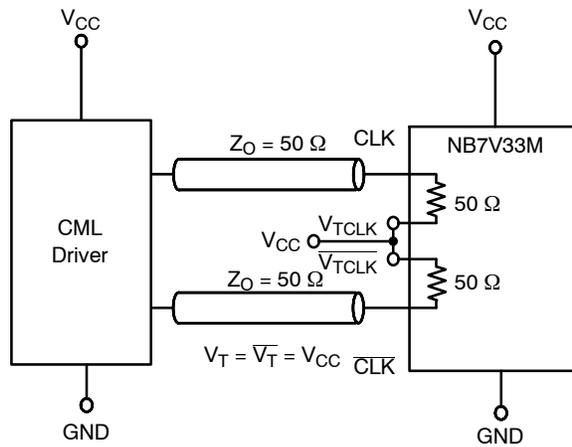


Figure 13. Standard 50 Ω Load CML Interface

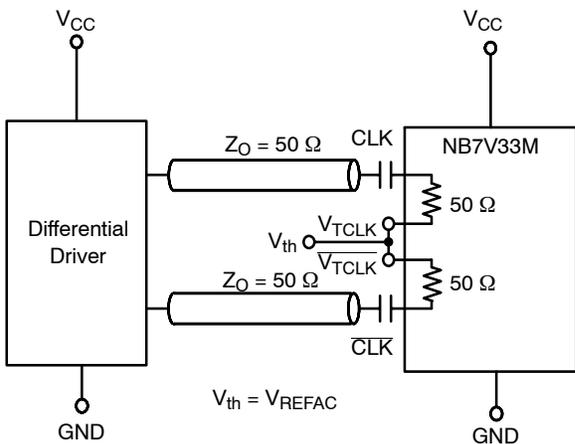


Figure 14. Capacitor-Coupled Differential Interface ($V_{TCLK}/\sqrt{V_{TCLK}}$ Connected to V_{REFAC} ; V_{REFAC} Bypassed to Ground with 0.1 μ F Capacitor)

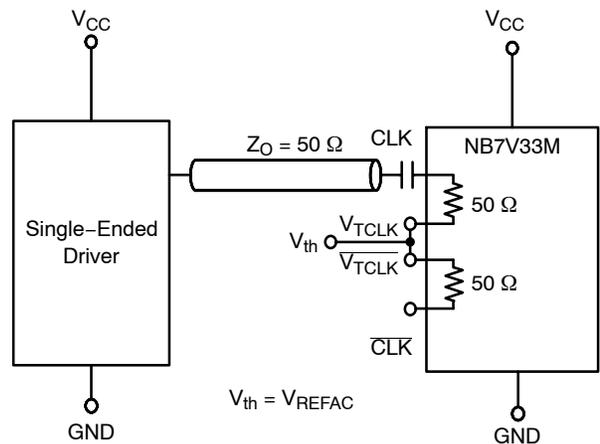


Figure 15. Capacitor-Coupled Single-Ended Interface ($V_{TCLK}/\sqrt{V_{TCLK}}$ Connected to V_{REFAC} ; V_{REFAC} Bypassed to Ground with 0.1 μ F Capacitor)

NB7V33M

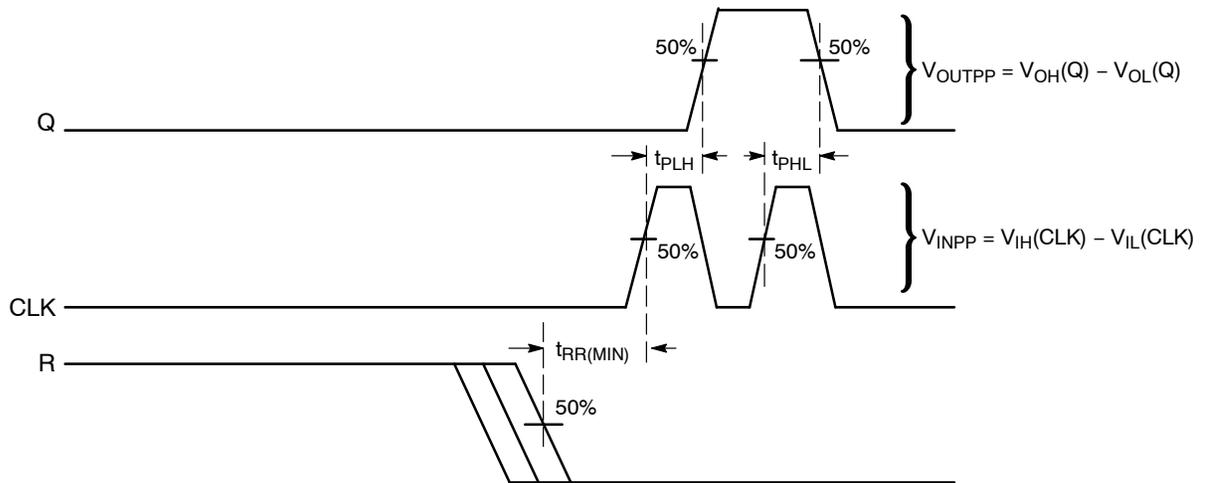


Figure 16. AC Reference Measurement (Timing Diagram)

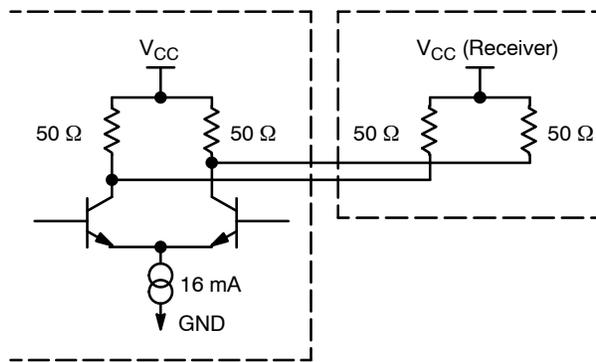


Figure 17. Typical CML Output Structure and Termination

NB7V33M

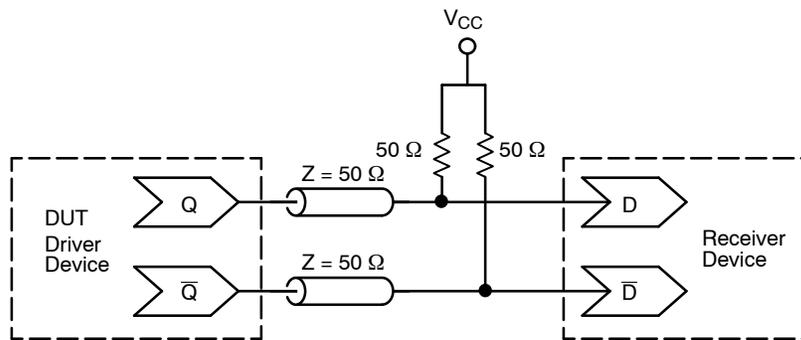


Figure 18. Typical Termination for CML Output Driver and Device Evaluation

DEVICE ORDERING INFORMATION¹

| Device | Package | Shipping [†] |
|---------------|---------------------|-----------------------|
| NB7V33MMNG | QFN-16 (Pb-Free) | 123 Units / Rail |
| NB7V33MMNHTBG | QFN-16 (Pb-Free) | 100 / Tape & Reel |
| NB7V33MMNTXG | QFN-16 (Pb-Free) | 3000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

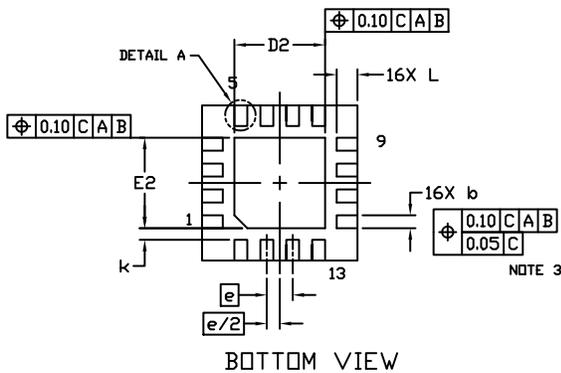
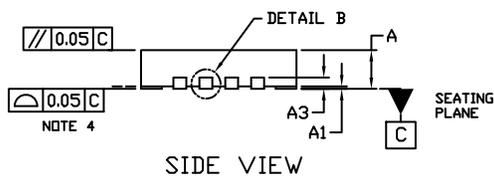
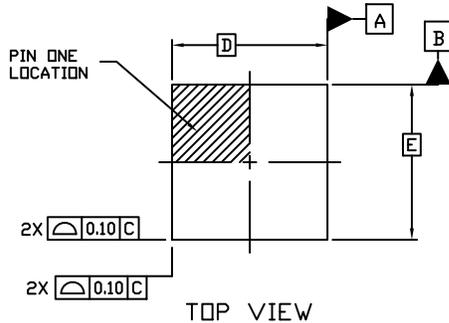
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

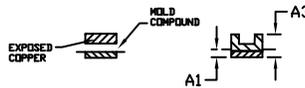
QFN16 3x3, 0.5P
CASE 485G
ISSUE G

DATE 08 OCT 2021

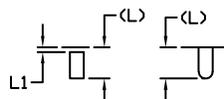


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



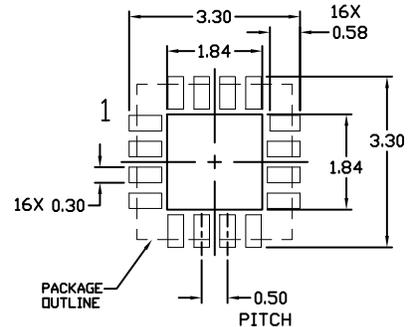
DETAIL B
ALTERNATE
CONSTRUCTIONS



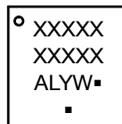
DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

| DIM | MILLIMETERS | | |
|----------|-------------|------|------|
| | MIN. | NDM. | MAX. |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.03 | 0.05 |
| A3 | 0.20 REF | | |
| <i>b</i> | 0.18 | 0.24 | 0.30 |
| D | 3.00 BSC | | |
| D2 | 1.65 | 1.75 | 1.85 |
| E | 3.00 BSC | | |
| E2 | 1.65 | 1.75 | 1.85 |
| <i>e</i> | 0.50 BSC | | |
| <i>k</i> | 0.18 TYP | | |
| L | 0.30 | 0.40 | 0.50 |
| L1 | 0.00 | 0.08 | 0.15 |

MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|-------------------------|------------------------|--|
| DOCUMENT NUMBER: | 98AON04795D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | QFN16 3X3, 0.5P | PAGE 1 OF 1 |

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[onsemi:](#)

[NB7V33MMNG](#) [NB7V33MMNTXG](#) [NB7V33MMNHTBG](#)